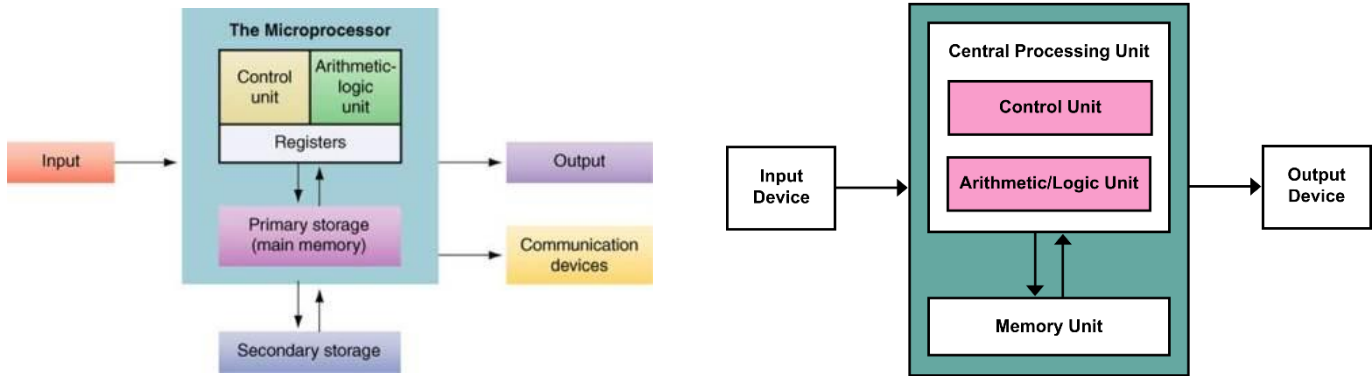


# Von Neumann Architecture



The Von Neumann architecture is a standard design of computer system with different entities connected over a bus.

- 1) Input/output or I/O Unit
- 2) A central processing unit (CPU)
- 3) Dedicated registers
- 4) Buses

## I/O Devices

Inputs are the signals or data received into the computer system from the outside world via input devices. The data is stored in internal registers.

Outputs are the signals or data returned from the computer system to the outside world via output devices. Together these peripheral devices form the I/O unit.

## The Processing unit

The CPU is responsible for carrying out the fetch-decode-execute cycle. The CPU fetches instructions and data from the RAM or cache, decodes then executes.

It is separated into the ALU (Arithmetic logic unit) and a Control Unit

## ALU

This calculates the arithmetic logic of instructions from programs (carries out calculations on the data) needed by programs. It can carry out simple calculations like adding/subtracting/multiplying/dividing and make logic operations like 'greater than' or 'less than' or 'equal to'. It also acts as a conduit for input and output to and from the processor.

## Control Unit,

This controls the flow of data through the processor. It manages the execution of machine code by sending control signals to the rest of the computer. Control signals are sent over the control bus to connected devices like hard drives and graphics cards. The control unit synchronises instructions to the internal clock speed. Some instructions can take less than one clock cycle to complete but the CPU will only start on the next instruction once the clock cycle is over. The control unit command for instructions and data to be fetched by assigning control signals to the memory registers. Once the instruction is decoded it sends more signals to the hardware to execute it (i.e. it tells the computers' memory, ALU and I/O devices how to respond to an instruction).

## Memory unit

The memory unit is responsible for fetching data and instructions from the main memory and pulling them into registers needed for the data to be processed. An instruction can only run on data within a register so the memory unit is responsible for fetching from and saving to memory. Therefore the memory unit makes use of what is known as the fetch-decode-execute cycle.

## Processor speed

This is measured by the **number of clock cycles** a processor **can perform per second** and is measured in hertz (Hz).

**Clock cycle** = One increment of the CPU clock (fetch-decode-execute a single instruction).

## Bus types

The bus is a set of parallel wires connecting two or more components of a computer. It typically consists of 8, 16, 32 or 64 lines. They connect all the components (I/O devices) to the CPU and RAM and allow the transfer of data between the components.

- **Address bus:** is used to identify locations in other components by transferring memory addresses to the either the memory or the I/O controller. Unidirectional flow. The address may be for a location of an instruction or piece of data to be fetched or stored.
- **Control bus** – is used to send signals that coordinate the flow of data and manage the activities of the peripheral devices. It transmits command, timing and specific status information between components.
- **Data bus** – transfers data and instructions between peripherals, memory and the CPU.

These 3 buses are commonly collectively called the system bus. Each bus is a shared transmission medium, so only one device can transmit along the bus at any given time.

(The von Neumann architecture has only one data bus so data transfers and instruction fetches are scheduled: They cannot run at the simultaneously).

The main idea the Von Neumann architecture introduced was that not only the data but also the program processing the data should also be stored in the memory. This made it easy to re-program the computer.

The control bus is bidirectional so signals can be transferred in both directions. The data and address buses are shared by all components in the system. Control lines must, therefore, be provided to ensure access and use of the data and address buses by different components does not conflict.

## EEPROM memory

'Electrically Erasable Programmable Read-Only Memory' is a type of non-volatile memory used in electronic devices to store relatively small amounts of data and allowing for individual bytes to be erased and reprogrammed.

**Von Neumann architecture** relies on the **stored program concept**:

*Machine code instructions are fetched and executed serially by a processor that can perform arithmetic and logic operations.*

*Two requirements for the stored program concept:*

- 1. A program must be resident in the memory to be executed*
- 2. The machine code instructions are fetched from the memory one at a time, decoded and executed by the processor.*

### **Other key features of Von Neumann**

- 1. In a Von Neumann machine, the same data bus is used for both instructions and data. It has a bidirectional flow.*
- 2. Similarly, a single address bus is used for the unidirectional transmission of address locations from the CPU to the memory or I/O controller.*
- 3. The same word length is used for all memory, whether it holds data or instructions.*